WHAT IS CLAIMED IS:

1. In an integrated circuit having a fully-decoded array of memory cells, each memory cell associated with one of a plurality of X-lines and one of a plurality of Y-lines, a method of operating the memory array comprising the steps of:

selecting at least a first Y-line;

in a first mode of operation, selecting an X-line associated with the first selected Y-line to impress a read bias across a corresponding memory cell coupled between the selected X-line and the first selected Y-line;

in a second mode of operation, selecting a first plurality of X-lines associated with the first selected Y-line to impress a read bias across each of a corresponding first plurality of selected memory cells respectively coupled between the first plurality of selected X-lines and the first selected Y-line;

in at least the second mode of operation:

enabling a first read circuit having an input coupled to the first selected Y-line; and

generating a first read signal on an output of the first read circuit having a first value if an aggregate read current of the first plurality of selected memory cells exceeds a second mode threshold level.

2. The invention defined by claim 1 further comprising the steps of:

in the first mode of operation:

enabling the first read circuit; and

generating the first read signal on the output of the first read circuit having a first value if a read current of the selected memory cell exceeds a first mode threshold level, and otherwise having a second value opposite the first value.

3. The invention defined by claim 2 wherein:

the second mode threshold level is different than the first mode threshold level.

4. The invention defined by claim 1 further comprising the steps of:

in the first mode of operation, enabling another read circuit, other than the first read circuit, having an input coupled to the first selected Y-line; and

generating a read signal on an output of the other read circuit having a first value if a read current of the selected memory cell exceeds a first mode threshold level, and otherwise having a second value opposite the first value.

5. The invention defined by claim 4 wherein:

the second mode threshold level is different than the first mode threshold level.

6. The invention defined by claim 1 further comprising:

in the second mode of operation, generating an output signal derived at least from the first read signal.

7. The invention defined by claim 1 further comprising the steps of:

in the second mode of operation:

selecting a second Y-line;

selecting a second plurality of X-lines associated with the second selected Y-line to impress a read bias across each of a corresponding second plurality of selected memory cells respectively coupled between the second plurality of selected X-lines and the second selected Y-line;

enabling a second read circuit having an input coupled to the second selected Y-line; and

generating a second read signal on an output of the second read circuit having a first value if an aggregate read current of the second plurality of selected memory cells exceeds a threshold level.

8. The invention defined by claim 7 wherein:

the first and second selected Y-lines are disposed in a single sub-array of the memory array.

9. The invention defined by claim 8 wherein:
the first and second plurality of selected X-lines are identical.

10. The invention defined by claim 7 wherein:
the first and second selected Y-lines are disposed in separate sub-arrays of the memory array.

11. The invention defined by claim 7 further comprising the steps of:
in the second mode of operation:
generating an output signal for indicating whether at least one of the first and second read signals is at its respective first value.

12. The invention defined by claim 7 further comprising the steps of:
in the second mode of operation:
generating an output signal having a first value if either one or both of the first and second read signals are at their respective first values, and having a second value otherwise.

13. The invention defined in claim 1 wherein:
the read bias in the first mode of operation is substantially the same as in the second mode of operation.

14. In an integrated circuit having a fully-decoded array of passive element memory cells, each memory cell comprising an anti-fuse and associated with one of a plurality of X-lines and one of a plurality of Y-lines, a method of operating the memory array comprising the steps of:
selecting at least a first Y-line;
in a first mode of operation, selecting an X-line associated with the first selected Y-line to impress a read bias across a corresponding memory cell coupled between the selected X-line and the first selected Y-line;
in a second mode of operation, selecting a first plurality of X-lines associated with the first selected Y-line to impress a read bias across each of a corresponding first plurality of selected memory cells respectively

coupled between the first plurality of selected X-lines and the first selected Y-line;

in both the first and second modes of operation:

enabling a first read circuit having an input coupled to the first selected Y-line;

generating a first read signal on an output of the first read circuit having a first value if an aggregate read current through the one or more selected memory cells exceeds a respective threshold level; and

generating an output signal derived at least from the first read signal.

15. The invention defined by claim 14 wherein:

the threshold level for the second mode of operation is different than for the first mode of operation.

16. The invention as recited in claim 14 wherein the step of selecting a first plurality of X-lines includes:

over-riding at least one address signal to cause an X-line decoder circuit to simultaneously select more than one X-line.

17. The invention defined by claim 14 further comprising the steps of:

in the second mode of operation:

selecting a second Y-line;

selecting a second plurality of X-lines associated with the second selected Y-line to impress a read bias across each of a corresponding second plurality of selected memory cells respectively coupled between the second plurality of selected X-lines and the second selected Y-line;

enabling a second read circuit having an input coupled to the second selected Y-line; and

generating a second read signal on an output of the second read circuit having a first value if an aggregate read current through the second plurality of selected memory cells exceeds the second mode threshold level.

18. The invention defined by claim 17 wherein:
the first and second selected Y-lines are disposed in separate sub-arrays of the memory array.

19. The invention defined by claim 17 further comprising the steps of:
in the second mode of operation:
generating an output signal having a first value if either one or both of the first and second read signals are at their respective first values, and having a second value if both the first and second read signals are at their respective second values.

20. The invention defined by claim 17 wherein:
the first and second selected Y-lines are disposed in a first sub-array of the memory array; and
the first and second plurality of selected X-lines are identical.

21. The invention defined by claim 20 further comprising the steps of:
in the second mode of operation:
selecting a third Y-line disposed in a second sub-array of the memory array different than the first sub-array;
selecting a third plurality of X-lines associated with the third selected Y-line to impress a read bias across each of a corresponding third plurality of selected memory cells respectively coupled between the third plurality of selected X-lines and the third selected Y-line;
enabling a third read circuit having an input coupled to the third selected Y-line; and
generating a third read signal on an output of the third read circuit having a first value if an aggregate read current through the third plurality of selected memory cells exceeds the second mode threshold level.

22. The invention defined by claim 21 further comprising the steps of:
in the second mode of operation:

generating an output signal for indicating whether at least one of the first, second, and third read signals is at its respective first value.

23. The invention defined by claim 21 further comprising the steps of:
in the second mode of operation:

generating a first output signal for indicating whether at least one of the first and second read signals is at its respective first value; and

generating a second output signal for indicating whether at least the third read signal is at its respective first value.

24. In an integrated circuit having a fully-decoded array of memory cells, each memory cell associated with one of a plurality of X-lines and one of a plurality of Y-lines, a method of operating the memory array comprising the steps of:

simultaneously selecting a plurality of memory cells arranged in at least one group of memory cells;

determining whether a read current greater than a particular value flows collectively through the selected memory cells in each respective group;

generating one or more output signals numbering less than the number of simultaneously selected memory cells, each respective output signal for indicating whether a read current greater than the particular value flows through one or more selected memory cells of each group of memory cells respectively associated therewith.

25. The invention defined by claim 24 wherein:
each memory cell of a respective group of memory cells is associated with a respective Y-line.

26. The invention defined by claim 24 wherein:
at least one output signal represents memory cells of more than one group.

27. The invention defined by claim 24 wherein:

at least one output signal represents memory cells of a single group.

28. The invention defined by claim 24 wherein:
the output signals number less than the number of groups; and
each output signal represents memory cells of more than one group.

29. An integrated circuit comprising:
a fully-decoded array of memory cells, each memory cell coupled to one of a plurality of X-lines and one of a plurality of Y-lines, wherein each Y-line is associated with a plurality of X-lines by virtue of the memory cells respectively coupled therebetween;
an X-line circuit for selecting, in a first mode of operation, an X-line associated with a first selected Y-line to impress a read bias across a corresponding memory cell coupled between the selected X-line and the first selected Y-line, and for selecting, in a second mode of operation, a first plurality of X-lines associated with the first selected Y-line to impress a read bias across each of a corresponding first plurality of selected memory cells respectively coupled between the first plurality of selected X-lines and the first selected Y-line;
a first read circuit for determining, in at least the second mode of operation, whether an aggregate read current of the first plurality of selected memory cells coupled to the first selected Y-line exceeds a second mode threshold level of current, and for generating a first read signal accordingly.

30. The invention defined by claim 29 wherein:
the first read circuit is configured for determining, in the first mode of operation, whether a read current of the selected memory cell coupled to the selected Y-line exceeds a first mode threshold level of current.

31. The invention defined by claim 30 wherein:
the threshold level of current for the first read circuit in the second mode of operation is different than for the first mode of operation.

32. The invention defined by claim 29 further comprising:

another read circuit different than the first read circuit for determining, in the first mode of operation, whether a read current of the selected memory cell coupled to the selected Y-line exceeds a first mode threshold level of current.

33. The invention defined by claim 32 wherein:

the threshold level of current for the first read circuit in the second mode of operation is different than the threshold level of current for the other read circuit in the first mode of operation.

34. The invention defined by claim 29 further comprising:

an output circuit responsive to at least the first read signal, for conveying an output signal derived at least from the first read signal.

35. The invention defined by claim 29 further comprising:

a second X-line circuit for selecting, in the second mode of operation, a second plurality of X-lines associated with a second selected Y-line to impress a read bias across each of a corresponding second plurality of selected memory cells respectively coupled between the second plurality of selected X-lines and the second selected Y-line; and

a second read circuit for determining, in at least the second mode of operation, whether an aggregate read current of the second plurality of selected memory cells coupled to the second selected Y-line exceeds a second mode threshold level of current, and for generating a second read signal accordingly.

36. The invention defined by claim 35 wherein:

the first and second selected Y-lines are disposed in a single sub-array of the memory array.

37. The invention defined by claim 36 wherein:

the first and second plurality of selected X-lines are identical.

38. The invention defined by claim 35 wherein:

the first and second selected Y-lines are disposed in separate sub-arrays of the memory array.

39. The invention defined by claim 35 further comprising:

a combining circuit responsive to at least the first and second read signals, for conveying an output signal derived at least from the first and second read signals.

40. An integrated circuit comprising:

a fully-decoded array of passive element memory cells, each memory cell comprising an anti-fuse and coupled to one of a plurality of X-lines and one of a plurality of Y-lines, wherein each Y-line is associated with a plurality of X-lines by virtue of the memory cells respectively coupled therebetween;

a first X-line circuit for selecting, in a read mode of operation, an X-line associated with a first selected Y-line to impress a read bias across a corresponding memory cell coupled between the selected X-line and the first selected Y-line, and for selecting, in a test mode of operation, a first plurality of X-lines associated with the first selected Y-line to impress the read bias across each of a corresponding first plurality of selected memory cells respectively coupled between the first plurality of selected X-lines and the first selected Y-line;

a first read circuit for determining, in both the read and test modes of operation, whether an aggregate read current of the one or more selected memory cells coupled to the selected Y-line exceeds a respective threshold level of current, and for generating a first read signal accordingly.

an output circuit coupled to receive at least the first read signal, for generating an output signal derived from at least the first read signal.

41. The invention defined by claim 40 wherein:

the threshold level of current for the test mode of operation is different than for the read mode of operation.

42. The invention as recited in claim 40 wherein the X-line circuit includes:

means for inhibiting at least one address signal to cause an X-line decoder circuit to simultaneously select more than one X-line.

43. The invention defined by claim 40 further comprising:

a second X-line circuit for selecting, in the second mode of operation, a second plurality of X-lines associated with a second selected Y-line to impress the read bias across each of a corresponding second plurality of selected memory cells respectively coupled between the second plurality of selected X-lines and the second selected Y-line; and

a second read circuit for determining, in at least the test mode of operation, whether an aggregate read current of the second plurality of selected memory cells coupled to the second selected Y-line exceeds the test mode threshold level of current, and for generating a second read signal accordingly;

wherein the first and second selected Y-lines are disposed in separate sub-arrays of the memory array.

44. The invention defined by claim 40:

wherein the first plurality of X-lines associated with the first selected Y-line are also associated with a second selected Y-line disposed with the first selected Y-line in a single sub-array of the memory array, said first X-line circuit also for impressing, during the test mode of operation, the read bias across each of a corresponding second plurality of selected memory cells respectively coupled between the first plurality of selected X-lines and the second selected Y-line; and

further comprising a second read circuit for determining, in at least the test mode of operation, whether an aggregate read current of the second plurality of selected memory cells coupled to the second selected Y-line exceeds a threshold level of current, and for generating a second read signal accordingly.

45. The invention defined by claim 40 wherein the first X-line circuit comprises:

a decoder circuit configurable during the read mode to select one of the plurality of X-lines by decoding a first group of address signals, and configurable during the test mode to select more than one of the plurality of X-lines by inhibiting a portion of the first group of address signals and decoding the remaining non-inhibited portion.

46. The invention defined by claim 45 wherein:

the inhibited portion represent contiguous low-order addresses, and the selected first plurality of X-lines during the test mode are contiguous in the memory array.

47. The invention defined by claim 40 wherein:

the memory array comprises a three-dimensional memory array having at least two planes of memory cells, each memory cell of a given plane coupled to one of a plurality of X-lines associated with the given plane and further coupled to one of a plurality of Y-lines associated with the given plane, wherein each Y-line is associated with a plurality of X-lines by virtue of the memory cells respectively coupled therebetween.

48. The invention defined by claim 47 wherein:

the first X-line circuit is configurable during the test mode to select at least one of a plurality of first layer X-lines associated with the first selected Y-line, and to select at least one of a plurality of second layer X-lines also associated with the first selected Y-line.

49. The invention defined by claim 47 wherein:

the first X-line circuit is configurable during the test mode to select at least one X-line associated with a respective one of two adjacent memory planes, each such selected X-line being also associated with the first selected Y-line.

50. An integrated circuit comprising:

a fully-decoded memory array of memory cells, each memory cell coupled to one of a plurality of X-lines and one of a plurality of Y-lines, wherein

each Y-line is associated with a plurality of X-lines by virtue of the memory cells respectively coupled therebetween;

means for simultaneously selecting a plurality of memory cells arranged in at least one group of memory cells;

means for determining whether an aggregate read current greater than a particular value flows through the selected memory cells in each respective group;

means for generating one or more output signals numbering less than the number of simultaneously selected memory cells, each respective output signal for indicating whether a read current greater than the particular value flows through one or more selected memory cells of each group of memory cells respectively associated therewith.

51. The invention defined by claim 50 wherein:

each memory cell of a respective group of memory cells is associated with a respective Y-line.

52. The invention defined by claim 50 wherein:

at least one output signal represents memory cells of more than one group.

53. The invention defined by claim 50 wherein:

at least one output signal represents memory cells of a single group.

54. The invention defined by claim 50 wherein:

the output signals number less than the number of groups; and

each output signal represents memory cells of more than one group.

55. A method for testing a fully-decoded memory array of programmable memory cells, the method comprising the steps of:

(a) identifying a maximum acceptable value of read current that would result from applying a given voltage across a defined group of unprogrammed memory cells;

(b) applying the given voltage across a first group of memory cells to be tested;

(c) sensing a current through the first group of memory cells from step (b); and

(d) comparing the current of step (c) with the value of step (a).

56. The invention defined by claim 55 further comprising the steps of:

(e) applying the given voltage across a second group of memory cells to be tested;

(f) sensing a current through the second group of memory cells from step (e); and

(g) comparing the current of step (f) with the value of step (a).

57. The invention defined by claim 56 wherein:

the first and second groups of memory cells are disposed in a single sub-array of the memory array.

58. The invention defined by claim 56 wherein:

the first and second groups of memory cells are disposed in separate sub-arrays of the memory array.

59. The invention defined by claim 55 further comprising the steps of:

generating an output signal to communicate the comparison of step (d).

60. The invention defined by claim 56 further comprising the steps of:

generating an output signal to jointly communicate the comparison of step (d) and the comparison of step (f).

61. The invention defined by claim 55 wherein:

the programmable memory cells comprise passive element memory cells.

62. The invention defined by claim 61 wherein:

the passive element memory cells comprise antifuse memory cells.

63. An integrated circuit comprising:

a fully-decoded memory array of programmable memory cells, each memory cell coupled to an associated X-line and an associated Y-line;

test mode

a first X-line circuit normally configured to select one of a first plurality of X-lines associated with a first selected Y-line but configurable, during a test mode, to select more than one of the X-lines associated with the first selected Y-line; and

a first Y-line sense circuit for sensing, when enabled, a read current on the first selected Y-line;

wherein, during the test mode, the X-line decoder is configured to select more than one of the first plurality of X-lines when the first Y-line sense circuit is enabled.

64. The invention defined by claim 63 wherein the first X-line circuit comprises:

a decoder circuit normally configurable to select one of the first plurality of X-lines by decoding a first group of address signals, and configurable during the test mode to select more than one of the plurality of X-lines by inhibiting a portion of the first group of address signals and decoding the remaining non-inhibited portion.

65. The invention defined by claim 64 wherein:

the inhibited portion represent contiguous low-order addresses for the X-line circuit, and the selected first plurality of X-lines during the test mode are contiguous in the memory array.

66. The invention defined by claim 63 wherein:

the memory array comprises a three-dimensional memory array having at least two planes of memory cells, each memory cell of a given plane coupled to one of a plurality of X-lines associated with the given plane and further coupled to one of a plurality of Y-lines associated with the given plane, wherein each Y-line is associated with a plurality of X-lines by virtue of the memory cells respectively coupled therebetween.

67. The invention defined by claim 63 further comprising:

an output for indicating whether a group of normally independently-decoded memory cells are unprogrammed.

68. The invention defined by claim 63 wherein:

the programmable memory cells comprise passive element antifuse memory cells.